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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,764	03/16/2004	Frederic Beaulieu	END920000020US3 (13427AB)	3431

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EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,764	BEAULIEU ET AL.	
	Examiner	Art Unit	
	Scott B. Geyer	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-18* is/are rejected.

7)☒ Claim(s) *19-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings submitted by the applicant on 3-16-04 are acceptable.

Claim Objections

Claims 16-21 are objected to because of the following informalities: Claims 16-21 depend upon claims which are not present in the instant application.

Appropriate correction is required.

On 6-23-04, the examiner discussed the dependency of claims 16-21 with the attorney of record, Mr. Leopold Presser. Mr. Presser informed the examiner that claims 16- 20 should depend from claim 15, and claim 21 should depend from claim 20. The claims have been treated as such for purposes of examination. However, an amendment of those claims is required in response to this office action to correct the errors.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Stearns et al. (6,160,705).

As to **claim 15**, Stearns et al. teach a substrate having first and second portions (first portion contains the chip and the second portion has the electrical wiring) as seen in figure 3, and the two portions are positioned relative to each other. The chip has a layer of circuitry on top of it, as evidenced by the wires 30,32,34 connecting to the to it's top area, as is also seen in figure 3. Power and ground connections are located on the second portion of the substrate, the ground 20 and power 18 connections being located in an interstitial pattern, as seen by figures 3 and 4. A signal connection (i.e. "ring") is also located on the second portion of the substrate and is adjacent the ground and power connection layers. Electrical connection is made between the chip and the power and ground connection layers using wire connectors having substantially the same height, as seen by figure 4. Electrical connection between the chip and the signal connection layer is made with a separate wire having a vertical height greater than that of the wires used to connect to the ground/power layers, as is also shown by figure 4.

As to **claim 16**, Stearns et al. teach a low profile chip package, comprising a substrate, a chip and connection wires, as shown by figures 3, 4 and 5.

As to **claim 17**, Stearns et al. teach a semiconductor chip located in a first portion of the substrate, and the active side of the chip is oriented "upward", as is depicted by figures 3-5. Therefore, Stearns et al. teach a "chip-up" configuration.

As to **claim 18**, Stearns et al. teach a semiconductor chip located in a first portion of the substrate, and the active side of the chip is oriented "upward", as is depicted by figures 3-5. However, if the device of Stearns et al. (as shown in a more completed state by figure 9) was oriented differently in three dimensional space, for

example flipped upside down, then the chip's active surface would be facing downward. At that point, Stearns et al. would teach a "chip-down" configuration. In other words, how a device is oriented in three dimensional space has no bearing on patentable, so Stearns et al. teach both a "chip-up" configuration, as detailed above for claim 17, and also teach a "chip-down" configuration for applicant's claim 18.

Allowable Subject Matter

Claims 19 and 20 are objected to as being dependent upon a rejected base claim, but **would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims** (emphasis added). The prior art of record and to the examiner's knowledge does not teach or render obvious, at least to the skilled artisan, the instant invention regarding:

the interstitial pattern of the ground and power planes comprising a simulated single ring configuration, as recited in claim 19, or

the particular positioning of a second signal ring and second power layer, combined with the electrical connections utilizing wires, as recited in claim 20. Claim 21 is dependent upon claim 20.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer whose telephone number is (571) 272-1958. The examiner can normally be reached on weekdays, between 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT GEYER
PATENT EXAMINER

SBG
June 24, 2004

David A. Zarneke
Primary Exam
6/26/04